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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,447	07/19/2001	Toshihiko Higuchi	81754.0064	2754
26021	7590	06/23/2003		
HOGAN & HARTSON L.L.P. 500 S. GRAND AVENUE SUITE 1900 LOS ANGELES, CA 90071-2611			EXAMINER	
			LE, THAO X	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 06/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	09/910,447	Applicant(s)	HIGUCHI, TOSHIHIKO
Examiner	Thao X Le	Art Unit	
		2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 10 April 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4,7,9,11,21-24,28,29 and 31-43 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-4,7,9,11,21-24,28,29 and 31-43 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 33, 37, 41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Recited limitation ' wherein the gate electrode is partially interposed between the first and second impurity layers' is unclear.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
- (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 1-4, 7, 9, 32, 34-36, 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6528847 to Liu.

Regarding to claim 1, Liu discloses a semiconductor device in fig. 1M comprising: a semiconductor substrate 12, column 4 line 39, having an indented region, Fig. 1D, a gate

dielectric layer 34, column 7 line 34, formed on the indented region, fig. 1E, a gate electrode 36/56, column 8 lines 17-20, formed on the gate dielectric layer 34, wherein a portion of the gate electrode is embedded in the semiconductor substrate 12 and another portion of the gate electrode is above the semiconductor substrate, first and second impurity diffusion layers 64, column 8 line 56, formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, a third impurity diffusion layer 30, fig. 1M, column 7 line 13, formed in a portion immediately below the gate electrode in the semiconductor substrate, and a sidewall dielectric layer 60, column 8 line 33, formed on the side surface section of the gate electrode, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, fig. 1M.

Regarding to claim 2, Liu discloses the semiconductor device wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric between about 0.05 – 0.25 μm (500 – 2500 \AA), column 6 line 63 (d_c).

Regarding to claim 3, Liu discloses a semiconductor device wherein the groove section 24, column 6 line 53, is formed at a specified location in the semiconductor substrate, and the gate electrode 36/56 is formed on a bottom surface of the groove section through the gate dielectric layer, fig 1M.

Regarding to claims 4, Liu discloses a semiconductor device wherein the gate electrode 36/56 is formed at least one alloy that includes at least two constituents selected from

polycrystalline silicon, tungsten, tantalum, copper and gold (36 = polysilicon, column 7 line 35 and 56 = tungsten column 8 line 18)

Regarding to claim 7, 9 Liu disclose a semiconductor device wherein the first and second impurity diffusion layers include an extension 32, column 7 line 34 fig. 1M, wherein a metal silicide layer 72 is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer 56 is formed on an upper surface thereof, fig. 1M column 8 lines 18 and 58

Regarding to claim 32, Liu discloses a semiconductor device in fig. 1M comprising: a semiconductor substrate 12, column 4 line 39, having an indented region, Fig. 1D, a gate dielectric layer 34, column 7 line 34, formed on the indented region, fig. 1E, a groove section formed at a specified location in the semiconductor substrate, fig. 1D, gate electrode 36/56, column 8 lines 17-20, formed on the gate dielectric layer 34, wherein a portion of the gate electrode is embedded in the semiconductor substrate 12 and another portion of the gate electrode is above the semiconductor substrate, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and a width of the upper surface of the gate electrode substantially equals the width of the groove, fig. 1M.

Regarding to claims 34-36, 42-43, Liu discloses a semiconductor device wherein the at least another portion of the gate electrode 56 is above the semiconductor substrate 12, and the first and second impurity diffusion regions 64, fig. 1M, wherein the third impurity diffusion layer 30 is completely disposed between the first and second impurity diffusion layers, wherein the extension region 32 of the first and second impurity diffusion layers are below the sidewall

dielectric layer 60, and wherein an area below the gate dielectric layer is free of the extension regions.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 11, 21-24, 28-29, 31, 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6528847 to Liu et al in view of US 6214679 to Murthy et al.

Regarding to claims 11, 21, Liu discloses a semiconductor device in fig. 1M comprising: a semiconductor substrate 12, column 4 line 39, having an indented region, Fig. 1D, a gate dielectric layer 34, column 7 line 34, formed on the indented region, fig. 1E, a gate electrode 36/56, column 8 lines 17-20, formed on the gate dielectric layer 34, wherein a portion of the gate electrode is embedded in the semiconductor substrate 12 and another portion of the gate electrode is above the semiconductor substrate, first and second impurity diffusion layers 64, column 8 line 56, formed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, a sidewall dielectric layer 60, column 8 line 33, formed on the side surface section of the gate electrode, wherein the gate electrode has a width that gradually increases from a bottom thereof toward an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, fig. 1M.

But Liu does not expressly disclose the semiconductor device wherein surfaces of the first and second impurity diffusion layers 64 are formed at a position higher than a surface of the element isolation region (STI).

But Murthy reference discloses the semiconductor device in fig. 12 wherein the surface of the first and second impurity diffusion layers 218 are formed at a position higher than a surface of the STI 204. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the elevated source and drain teaching of Murthy with Liu's device, because it would have increased the conductivity and good punch through characteristics obtained as taught by Murthy, column 5 line 62-67.

Regarding to claim 22, Liu discloses the semiconductor device wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric between about 0.05 – 0.25 μm (500 – 2500 \AA), column 6 line 63 (d_c).

Regarding to claim 23, Liu discloses a semiconductor device wherein the groove section 24, column 6 line 53, is formed at a specified location in the semiconductor substrate, and the gate electrode 36/56 is formed on a bottom surface of the groove section through the gate dielectric layer, fig 1M.

Regarding to claims 24, Liu discloses a semiconductor device wherein the gate electrode 36/56 is formed at least one alloy that includes at least two constituents selected from polycrystalline silicon, tungsten, tantalum, copper and gold (36 = polysilicon, column 7 line 35 and 56 = tungsten column 8 line 18)

Regarding to claim 28-29, 31 Liu disclose a semiconductor device wherein a third impurity diffusion layer 30, fig. 1M, column 7 line 13, formed in a portion immediately below the gate electrode in the semiconductor substrate, wherein a metal silicide layer 72 is formed on the first and second impurity diffusion layers, and the gate electrode includes a metal silicide layer 56 is formed on an upper surface thereof, fig. 1M column 8 lines 18 and 58, wherein the sidewall dielectric layer 60 has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and film thickness that gradually reduces from a bottom thereof toward an upper surface thereof, fig. 1M.

Regarding to claims 38-40, Liu discloses a semiconductor device wherein the at least another portion of the gate electrode 56 is above the semiconductor substrate 12, and the first and second impurity diffusion regions 64, fig. 1M, wherein the third impurity diffusion layer 30 is completely disposed between the first and second impurity diffusion layers, wherein the extension region 32 of the first and second impurity diffusion layers are below the sidewall dielectric layer 60, and wherein an area below the gate dielectric layer is free of the extension regions.

Response to Arguments

7. Applicant's arguments filed on 04/10/03 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Art Unit: 2814

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
June 6, 2003

Caonhnh
PHAT X. CAO
PRIMARY EXAMINER